(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 881 622 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
02.12.1998 Bulletin 1998/49

(51) Int Cl.[6]: **G09G 3/36**

(21) Application number: **98303688.0**

(22) Date of filing: **12.05.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **27.05.1997 JP 136801/97**

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(54) Power-off screen clearing circuit for active matrix liquid crystal display

(57) A liquid crystal display comprising gate lines (32) to which the gates of the transistors (31a) in active switching elements (31) are connected, a node A supplied with a gate low voltage Vgl generated from a source voltage Vdd, a charge storage means (36) for storing a predetermined charge, a P-channel transistor (37) connected between the node A and the charge storage means (36), a node C connected to the gate of the P-channel transistor (37), a voltage supply means (38) for supplying the node C with a voltage causing the P-channel transistor (37) to be maintained in a high-resistance state while the source voltage Vdd is supplied to the liquid crystal display, a voltage reducing means (39) for using a capacitive coupling to reduce the voltage of the node C to a voltage causing the P-channel transistor (37) to become a low-resistance state in response to the change in the source voltage Vdd if the supply of the source voltage Vdd is stopped, and a control means (33) for supplying the charge stored in the charge storage means (36) to the gate lines (32) through the node A in response to the P-channel transistor (37) having become a low-resistance state, thereby to cause the transistors (31a) in active switching elements (31) to become a low-resistance state.

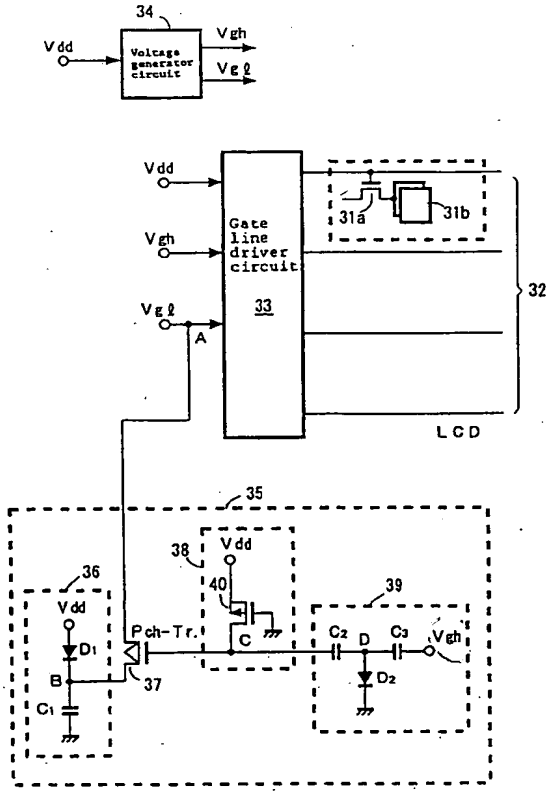

FIG. 3

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Description

The present invention relates to a liquid crystal display.

A TFT type Liquid Crystal Display (LCD) having active switching elements has a structure in which many active switching elements are arranged in a matrix. Figure 1 shows an equivalent circuit of such TFT. One end of the TFT is connected to a data line, and the other end is connected to a pixel voltage terminal Vp. The TFT gate is connected to a gate line N, and the TFT is selectively turned on/off in response to the signal provided to the gate line N. Further, the pixel voltage terminal vp is connected to a voltage terminal VCOM through a liquid crystal capacitance CLC and connected to a gate line N-1 through a secondary capacitance CS.

Generally, the output from a driver circuit for driving such panel is interrupted simultaneously with the turning-off of the power. Thus, even if the power is turned off to eliminate the display on a screen, sometimes an afterimage like a black spot is seen on the screen for a certain time. The occurrence of such afterimage is caused by the charge held on a load capacitance comprised of the liquid crystal capacitance CLC and the secondary capacitance CS. That is, while the charge is naturally discharged after the power is turned off, it is made visible on the screen by a reflected light as if it is written. Since the degree of the afterimage made visible by the reflected light increases as Aperture ratio of the TFT type LCD increases, it is a problem from the viewpoint of the display screen quality.

To solve the problem of the afterimage display, it is only required that, when the power is turned off, all the gate lines (all the unselected gate lines) supplied with a gate low voltage (for instance, -10 V,) by a gate line driver circuit be supplied with a voltage of the order of +2 V for a certain time period ever after the turning-off of the power. Since the TFTs in the corresponding active switching elements are caused to become a low-resistance state (on-state) by providing a voltage to the unselected gate lines to such extent, the charge in the pixel capacitance can forcibly be discharged to the gate lines on the instant. Accordingly, it is possible to instantaneously clear the afterimage.

As a background art related to this problem, there is Published Unexamined Japanese Patent Application No. 1-170986. This is to automatically detect the power-off of a liquid crystal display, and based on that, the TFT of the liquid crystal display element is held to be on for a predetermined time so that the stored charge of the pixel capacity can be discharged in a short time. As shown in the block diagram of Figure 2, by a source voltage VI supplied to a terminal 1 from the main body of a liquid crystal display, a capacitor 2b of a large capacitance is charged through a diode 2a. The source voltage VI is also supplied to a gate bus driver circuit 3. This source voltage holding circuit 2 is to hold the power of the operation power supply provided to a liquid crystal display panel for a predetermined time even after the power to the liquid crystal display is turned off. A voltage drop detection circuit 4 is to detect the voltage drop of the source voltage VI, and simultaneously holds the outputs of the gate bus driver circuit 3 at an active level for a predetermined time in response to the detected signal. That is, in this method, when the system power VI is turned off, the power within the LCD panel is not immediately turned off, but, first the voltage drop from the system is detected and a voltage supply circuit for rising the gate voltage is operated. Thereafter, after the afterimage on the screen is removed, to turn off the main power to the LCD panel, instructions are sent to the power circuit to finally turn off the power.

However, the background art has the following problems. First, since the source voltage VI is supplied to the gate bus driver circuit 3 through the diode 2a, a voltage drop occurs in the diode 2a. To solve the disadvantage due to the voltage drop, the above publication includes a description that the voltage VI itself may be made larger or a DC-DC converter may be provided on the input side of the power holding circuit 2 to increase the voltage. However, it cannot be denied that the circuit design is made complicated by the provision of such circuit.

Further, as a larger problem, it is required to reserve a power supply for operating circuits such as a circuit for detecting the turn-off of the system power, or an afterimage removal power hold/supply circuit and a power turn-off request/enable circuit after the afterimage removal, which are needed in the above art, after the system power VI is turned off. However, the circuit construction therefor is complex and expensive.

Accordingly, it is an object of the present invention to effectively remove the afterimage display after the turn-off of the power, which is due to the load capacitance in the TFT type LCD. It is preferred that such an object be achieved by means of a simple circuit construction.

According to a first aspect, the present invention provides a liquid crystal display in which many active switching elements are arranged in a matrix, each of the active switching elements has a transistor, and an afterimage occurring when the supply of the source voltage is stopped is removed, the liquid crystal display comprising: gate lines connected to the gates of the transistors in the active switching elements; a first node supplied with a second source voltage generated from the source voltage; charge storage means for storing a predetermined charge; a P-channel transistor connected between the first node and the charge storage means; a second node connected to the gate of the P-channel transistor; voltage supply means for supplying the second node with a voltage causing the P-channel transistor to be maintained in a high-resistance state while the source voltage is supplied to the liquid crystal display; voltage reducing means for using a capacitive coupling to reduce the voltage of the second node to a voltage

causing the P-channel transistor to become a low-resistance state in response to the change in the source voltage if the supply of the source voltage of the liquid crystal display is stopped; and control means for supplying the charge stored in the charge storage means to the gate lines through the first node in response to the P-channel transistor having become a low-resistance state, thereby to cause the transistors in the active switching elements to become a low-resistance state.

A second aspect of the present invention is related to a method for controlling the afterimage removing circuit provided in a liquid crystal display in which many active switching elements are arranged in a matrix, each of the active switching elements has a transistor, and gate lines are connected to the gates of the transistors in the active switching elements. The afterimage removing circuit comprises a first node for supplying a second source voltage generated from the source voltage and lower than the source voltage, a charge storage circuit for storing a predetermined charge, and a P-channel transistor connected between the first node and the charge storage means and having the gate thereof connected to a second node. To remove the afterimage occurring when the supply of the source voltage is stopped, the afterimage removing circuit is controlled as follows.

(a) A step of supplying the second node with a voltage causing the P-channel transistor to be maintained in a high-resistance state while the source voltage is supplied to the liquid crystal display.

(b) A step of using a capacitive coupling to reduce the voltage of the second node to a voltage causing the P-channel transistor to become a low-resistance state in response to the change in the source voltage if the supply of the source voltage of the liquid crystal display is stopped.

(c) A step of supplying the stored predetermined charge to the gate lines through the first node in response to the P-channel transistor having become a low-resistance state, thereby to cause the transistors in the active switching elements to become a low-resistance state.

In such arrangement, the control for supplying the charge stored in the charge storage means to a gate line is performed by the P-channel transistor as a switching element. First, while the power is on, a voltage is supplied so as to cause the P-channel transistor to be turned off. Since the source voltage rapidly changes from a certain value to zero if the power is turned off, a capacitive coupling can be used to turn on the P-channel transistor. By causing the potential of the gate line to rise by the charge stored in the charge storage means to cause the transistor in the active switching element to become a low-resistance state (generally, on-state), the charge stored in the element can instantaneously be discharged.

A preferred embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is an equivalent circuit of the TFT;

Figure 2 is a block diagram for explaining the background art;

Figure 3 is a schematic circuit diagram of the liquid crystal display in the present embodiment; and

Figure 4 is a circuit diagram showing another embodiment of the voltage supply circuit.

Figure 3 is a schematic circuit diagram of the liquid crystal display in the present embodiment. In the TFT type LCD, many active switching elements 31 are arranged in a matrix. Each active switching element consists of an FET 31a and opposed pixel electrodes 31b. The gate of each FET 31a is connected to a gate line 32, and its source is connected to a source line, not shown. A gate line driver circuit 33 is to selectively select desired gate lines, and to the selected gate lines, a gate high voltage Vgh, a third source voltage, is supplied. And, to all the other gate lines which are not selected (unselected gate lines), a gate low voltage Vgl, a second source voltage, is supplied. A voltage generation circuit 34 is to generate various voltages such as the gate high voltage Vgh (e.g. +20 v) and the gate low voltage Vgl (e.g. -10 V) if the external power supplied to the liquid crystal display is a single source voltage vdd (e.g. +5 V).

If the source voltage vdd is supplied to the liquid crystal display, the gate low voltage Vgl is supplied to a node A, and the gate line driver circuit 33 operates under the source voltages such as the source voltage vdd, the gate high voltage Vgh, and the gate low voltage Vgl which is the potential of the node A. An afterimage circuit 35 comprises a charge storage circuit 36, a P-channel transistor 37, a voltage supply circuit 38, and a voltage reducing circuit 39.

In the charge storage circuit 36, a diode D1 and a capacitance are serially connected between a source voltage terminal Vdd and a ground potential terminal Vss. And, when the power for the liquid crystal display is on (vdd is supplied), a predetermined charge is stored in the capacitance C1 through the diode D1. The capacitance C1 is set to a capacity which can cause the potential of a plurality of unselected gate lines to rise to a predetermined potential (e.g. about +2 V).

The drain of the P-channel transistor 37 is connected to the node A, the source is connected to a node B in the charge storage circuit 36, and the gate is connected to a node C in the voltage supply circuit 38. The transistor 37, described below in detail, is a switching element which is off (high-resistance state) when the power

is on, and changes to on (low-resistance state) when the power is turned off. Accordingly, it supplies a charge to unselected gate lines through the gate line driver circuit 33 only when the power is turned off.

The voltage supply circuit 38 is a P-channel transistor 40 provided between the source voltage terminal Vdd and the node C, and its gate is fixedly supplied with the ground potential. With this, when the power is on, the voltage of the node C is maintained at a voltage causing the P-channel transistor 37 to be turned off.

The voltage reducing circuit 39 consists of two capacitances C2 and C3, and a diode D2. The capacitance C2 is provided between the node C and a node D, and the capacitance C3 is provided between the node D and a gate high potential terminal Vgh. And, the diode D2 is forward-connected in the ground direction from the node D. As long as the gate high potential voltage Vgh is stable when the power is on, the potential of the node D is zero, and it has no effect on the potential of the node C which is stabilized by the voltage supply circuit 38.

Now, description is made to the operation for the case in which the supply of the power to the liquid crystal display is stopped. In this case, the source voltage Vdd instantaneously changes to zero. Thus, not only the source voltage Vdd, but also the high gate voltage Vgh and the low gate voltage Vgl generated therefrom instantaneously change to zero. Accordingly, this causes the potential of the source voltage terminal Vdd in the charge storage circuit 36 to become zero, but, since the diode D1 is connected, the charge in the capacitance C1 is not discharged to the source voltage terminal vdd side (which has changed to zero).

The source voltage terminal vdd in the voltage supply means 38 also becomes zero, but, since the potential of the node C in a floating state is higher, the potential of the node C is not decreased by the P-channel transistor 40. However, since the potential of the gate high voltage terminal Vgh in the voltage reducing circuit 39 instantaneously becomes zero (for instance, changes from +20 V to 0 V), the potential of the node C is made to drop at a time by the capacitive coupling between the capacitances C2 and C3, thereby to turn on the P-channel transistor 37. As a result, the potential of the node A is risen by the charge stored in the capacitance C1, and that voltage is supplied to the gate line driver circuit 33.

Consequently, the potential of a plurality of gate lines 31 unselected by the gate line driver circuit 33 rises (e.g. about +2 V), turning on the FET 31a in the active switching element 31 (low-resistance state) . This causes the charge stored in the element 31 to be forcibly discharged, for instance, to a source line. Since the charge stored in the active switching element 31 can forcibly be discharged, it is possible to erase the displayed afterimage faster than the case in which it is naturally discharged.

Thus, in the present embodiment, using the instantaneous change in the source voltage which occurs when the power is turned off, and the capacitive coupling in the voltage reducing circuit, the switching of the P-channel transistor is performed to execute the elimination of the afterimage. Accordingly, there are advantages that it is not necessary to reserve a special power supply for the operation after the turn-off of the system power, which was required in the background art, and that only a very simple and inexpensive circuit construction is needed.

The above description has been made to the case in which the afterimage removing circuit 35 is provided on the terminal side of the gate low voltage supplied to the gate line driver circuit 33. However, the present invention is not limited to this, and it is to be understood that it may be provided directly on the gate line 32 side without through the gate line driver circuit 33.

Further, the voltage supply circuit 38 may be constructed as shown in Figure 4. By providing a resistor in parallel with a diode in this way, the timing of turning on the P-channel transistor 37 can controlled more easily.

Thus, in accordance with the present invention, the afterimage occurring when the power is turned off can be eliminated with a very simple and inexpensive circuit construction, without reserving a special power supply for operating the circuit after the turn-off of the system power.

Claims

1. A liquid crystal display having a plurality of active switching elements arranged in a matrix, each of the active switching elements having a transistor and gate lines connected to gates of the transistors in the active switching elements the liquid crystal display comprising:

   a first node supplied with a second source voltage generated from the source voltage;

   charge storage means for storing a predetermined charge;

   a P-channel transistor connected between the first node and the charge storage means;

   a second node connected to the gate of the P-channel transistor;

   voltage supply means for supplying the second node with a voltage causing the P-channel transistor to be maintained in a high-resistance state while the source voltage is supplied to the liquid crystal display;

   voltage reducing means for using capacitive coupling to reduce the voltage of the second node to a voltage causing the P-channel tran-

sistor to become a low-resistance state in response to the change in the source voltage if the supply of the source voltage of the liquid crystal display is stopped; and

control means for supplying the charge stored in the charge storage means to the gate lines through the first node in response to the P-channel transistor having become a low-resistance state, thereby to cause the transistors in the active switching elements to become a low-resistance state.

2. A liquid crystal display as set forth in claim 1, wherein the control means comprises a gate line driver circuit for selectively selecting desired the gate lines, and the gate line driver circuit supplies the charge stored in the charge storage means to a plurality of unselected the gate lines other than the selected gate line through the first node.

3. A liquid crystal display as set forth in claim 1, wherein the second source voltage is a gate low voltage generated from the source voltage of the liquid crystal display.

4. A liquid crystal display as set forth in claim 3, wherein the control means are a gate line driver circuit, and the transistors in a plurality of the active switching elements which are supplied with the gate low voltage by the gate line driver circuit is caused to become a low-resistance state by the charge stored in the charge storage means.

5. A liquid crystal display as set forth in claim 3, wherein the voltage reducing means have a first capacitance having one end thereof connected to the second node and having the other end thereof connected to a third node, and a second capacitance having one end thereof supplied with a third source voltage and having the other end thereof connected to the third node.

6. A liquid crystal display as set forth in claim 5, wherein the third source voltage is a gate high voltage generated from the source voltage of the liquid crystal display and higher than the gate low voltage.

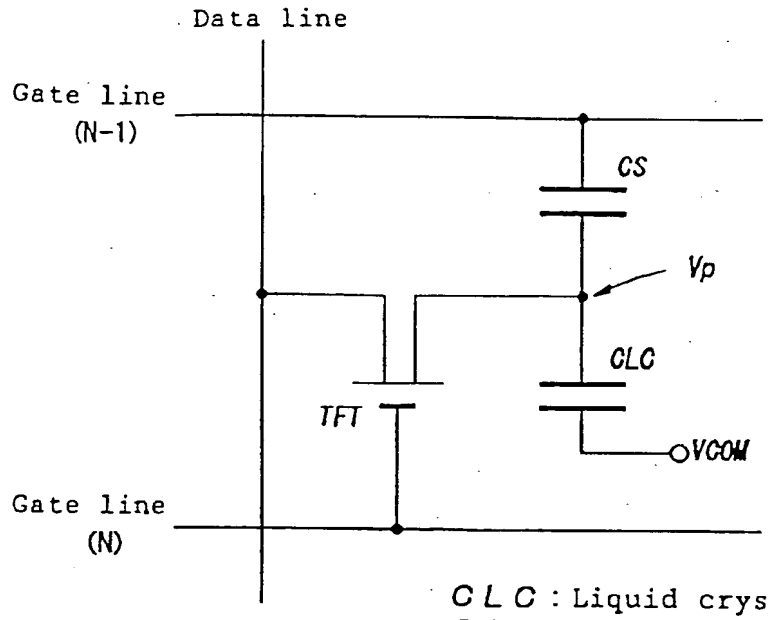
7. A liquid crystal display as set forth in claim 5, wherein the voltage reducing means have a diode which is forward-connected from the third node toward the ground potential terminal.

8. A method for controlling afterimage in a liquid crystal display comprising a plurality of active switching elements arranged in a matrix, each of the active switching elements having a transistor, and gate lines connected to the gates of the transistors in the active switching elements, the liquid crystal display further comprising an afterimage removing circuit, the afterimage removing circuit further having a first node, a charge storage circuit, and a P-channel transistor, the first node being supplied with a second source voltage generated from the source voltage and lower than the source voltage, the charge storage storing a predetermined charge; and, the P-channel transistor being connected between the first node and the charge storage circuit, and having the gate thereof connected to a second node, the method comprising the steps of:

supplying the second node with a voltage causing the P-channel transistor to be maintained in a high-resistance state while the source voltage is supplied to the liquid crystal display;

reducing, if the supply of the source voltage of the liquid crystal display is stopped, the voltage of the second node to a voltage causing the P-channel transistor to become a low-resistance state in response to the change in the source voltage by using a capacitive coupling; and

supplying the stored predetermined charge to the gate lines through the first node in response to the P-channel transistor having become a low-resistance state, thereby to cause the transistors in the active switching elements to become a low-resistance state.



CLC : Liquid crystal capacitance
CS : Secondary capacitance
Vp : Pixel voltage

FIG. 1

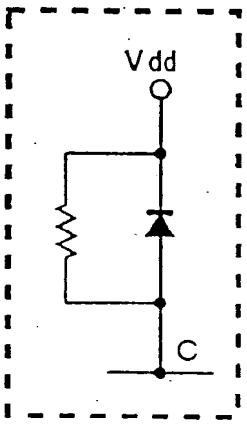


FIG. 4

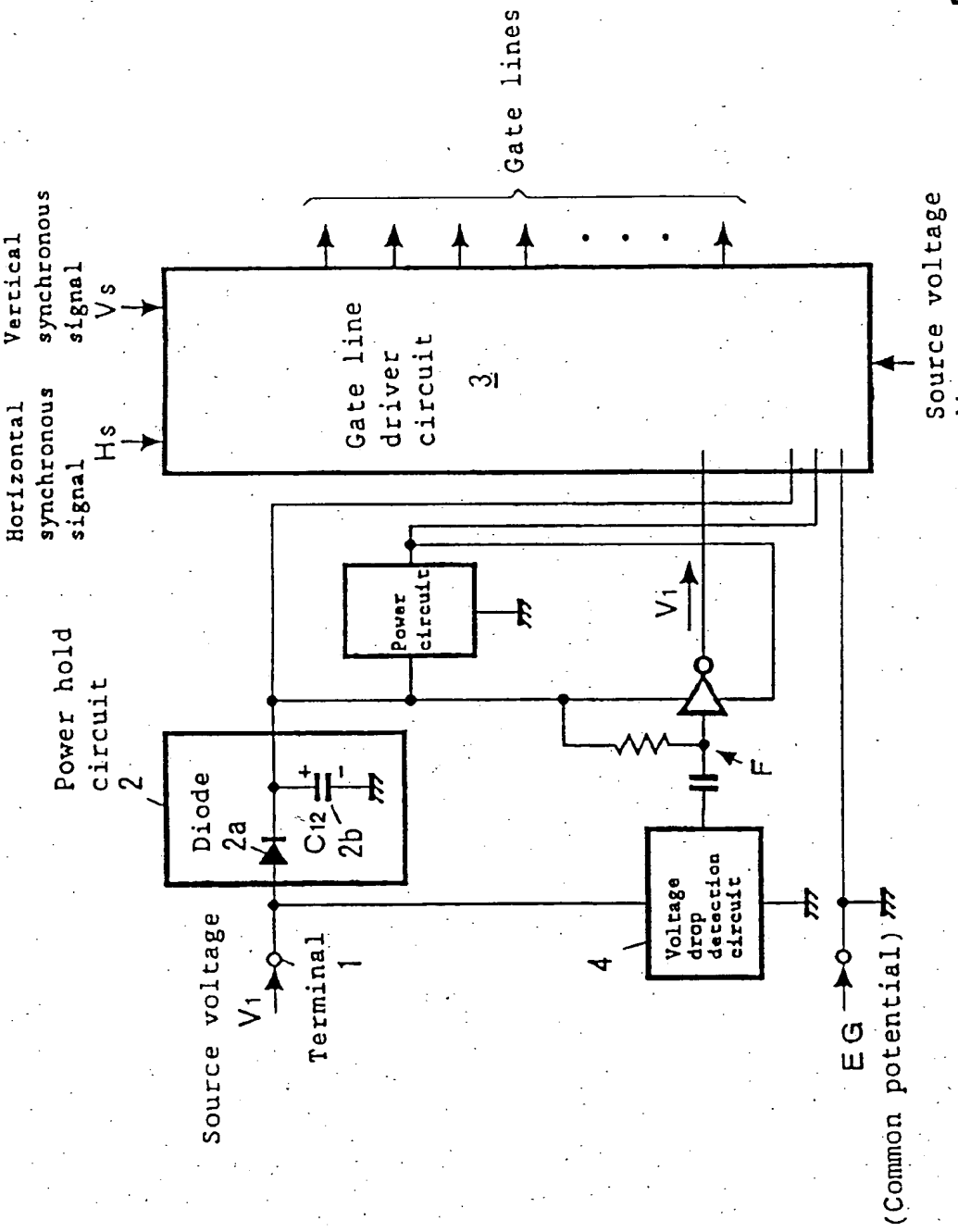

Gate lines
Vertical synchronous signal Vs
Horizontal synchronous signal Hs
Gate line driver circuit 3
Source voltage V3
Power circuit
V1
F
Power hold circuit 2
Diode 2a
C12 2b
Voltage drop detection circuit 4
Source voltage V1
Terminal 1
EG (Common potential)

FIG. 2

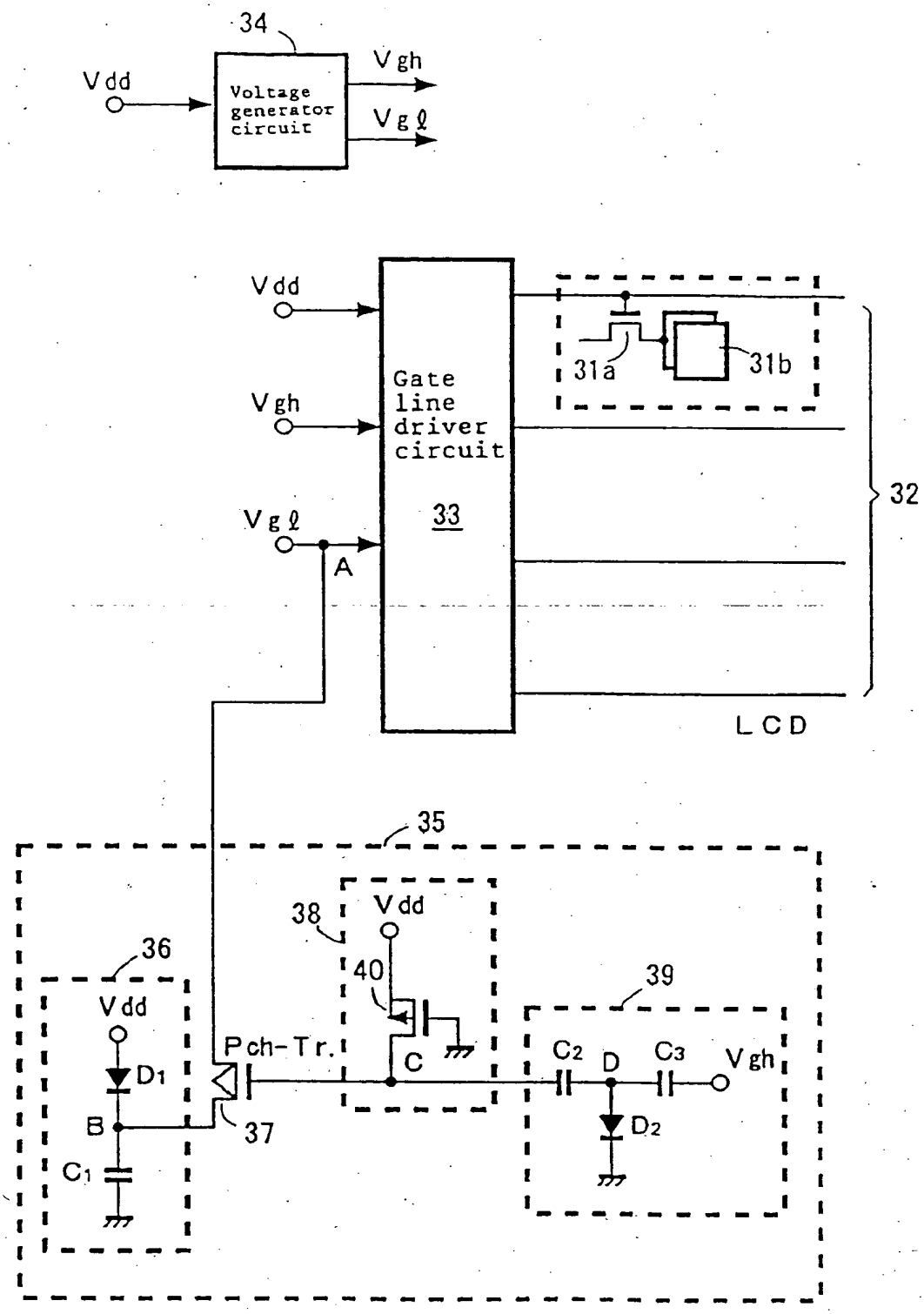

34
Vdd
Voltage generator circuit
Vgh
Vgℓ
Vdd
Vgh
Vgℓ
A
Gate line driver circuit
33
31a
31b
32
LCD
35
36
Vdd
D1
B
C1
37
Pch-Tr.
38
Vdd
40
C
39
C2
D
C3
Vgh
D2

FIG. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 3688

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	EP 0 764 932 A (SAMSUNG ELECTRONICS CO LTD) 26 March 1997 * column 3, line 12 - column 5, line 10; figures 4,6 *	1-4,8	G09G3/36
D,Y	EP 0 364 590 A (HOSIDEN ELECTRONICS CO) 25 April 1990 * abstract; figure 5 *	1-4,8	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 September 1998	Amian, D

CATEGORY OF CITED DOCUMENTS

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